National Semiconductor

December 1994

54F/74F544
Octal Registered Transceiver

General Description

The 'F544 octal transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable and Output Enable inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow. The A outputs are guaranteed to sink 24 mA (20 mA Mil) while the B outputs are rated for 64 mA (48 mA Mil). The 'F544 inverts data in both directions.

Features

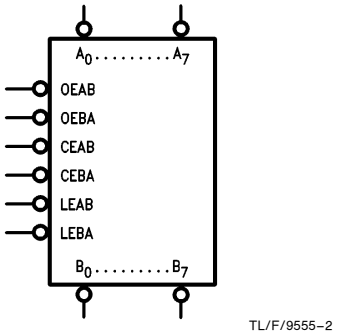
- 8-bit octal transceiver
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- A outputs sink 24 mA (20 mA Mil), B outputs sink 64 mA (48 mA Mil)
- 300 mil slim PDIP

Commercial	Military	Package Number	Package Description
74F544SPC		N24C	24-Lead (0.300″ Wide) Molded Dual-In-Line
	54F544DM (Note 2)	J24A	24-Lead Ceramic Dual-In-Line
	54F544SDM (Note 2)	J24F	24-Lead (0.300″ Wide) Ceramic Dual-In-Line
74F544SC (Note 1)		M24B	24-Lead (0.300″ Wide) Molded Small Outline, JEDEC
74F544MSA (Note 1)		MSA24	24-Lead Molded Shrink Small Outline, EIAJ, Type II
	54F544FM (Note 2)	W24C	24-Lead Cerpack
	54F544LM (Note 2)	E28A	24-Lead Ceramic Leadless Chip Carrier, Type C

Note 1: Devices also available in 13″ reel. Use suffix = SCX and MSAX.

Note 2: Military grade device with environmental and burn-in processing. Use suffix = DMQB, FMQB and LMQB

Logic Symbols



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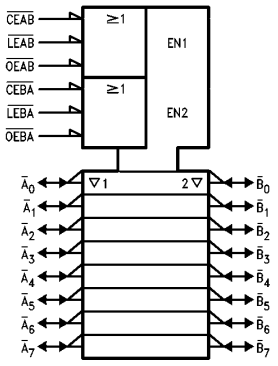
IEEE/IEC



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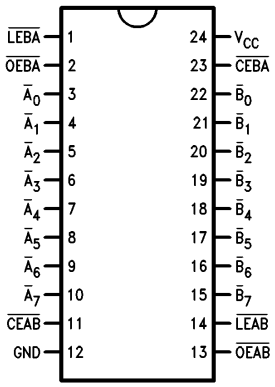
Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



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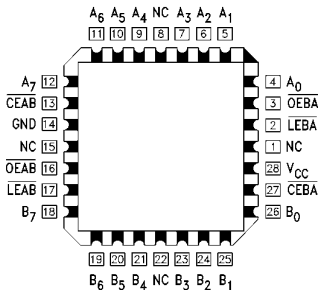
Pin Assignment for LCC



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Unit Loading/Fan Out

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)	1.0/1.0	20 μA/−0.6 mA
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)	1.0/1.0	20 μA/−0.6 mA
$\overline{CEAB}$	A-to-B Enable Input (Active LOW)	1.0/2.0	20 μA/−1.2 mA
$\overline{CEBA}$	B-to-A Enable Input (Active LOW)	1.0/2.0	20 μA/−1.2 mA
$\overline{LEAB}$	A-to-B Latch Enable Input (Active LOW)	1.0/1.0	20 μA/−0.6 mA
$\overline{LEBA}$	B-to-A Latch Enable Input (Active LOW)	1.0/1.0	20 μA/−0.6 mA
$\overline{A}_0$–$\overline{A}_7$	A-to-B Data Inputs or	3.5/1.083	70 μA/−650 μA
	B-to-A TRI-STATE Outputs	150/40(33.3)	−3 mA/24 mA (20 mA)
$\overline{B}_0$–$\overline{B}_7$	B-to-A Data Inputs or	3.5/1.083	70 μA/−650 μA
	A-to-B TRI-STATE Outputs	600/106.6(80)	−12 mA/64 mA (48 mA)

Functional Description

The 'F544 contains two sets of eight D-type latches, with separate input and output controls for each set. For data flow from A to B, for example, the A-to-B Enable ($\overline{CEAB}$) input must be LOW in order to enter data from $\overline{A}_0$–$\overline{A}_7$ or take data from $\overline{B}_0$–$\overline{B}_7$, as indicated in the Data I/O Control Table. With $\overline{CEAB}$ LOW, a LOW signal on the A-to-B Latch Enable ($\overline{LEAB}$) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the $\overline{LEAB}$ signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{CEAB}$ and $\overline{OEAB}$ both LOW, the TRI-STATE® B output buffers are active and reflect the data present at the output of the A latches. Control of data flow from B to A is similar, but using the $\overline{CEBA}$, $\overline{LEBA}$ and $\overline{OEBA}$ inputs.

Data I/O Control Table

Inputs			Latch Status	Output Buffers
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$		
H	X	X	Latched	High Z
X	H	X	Latched	—
L	L	X	Transparent	—
X	X	H	—	High Z
L	X	L	—	Driving

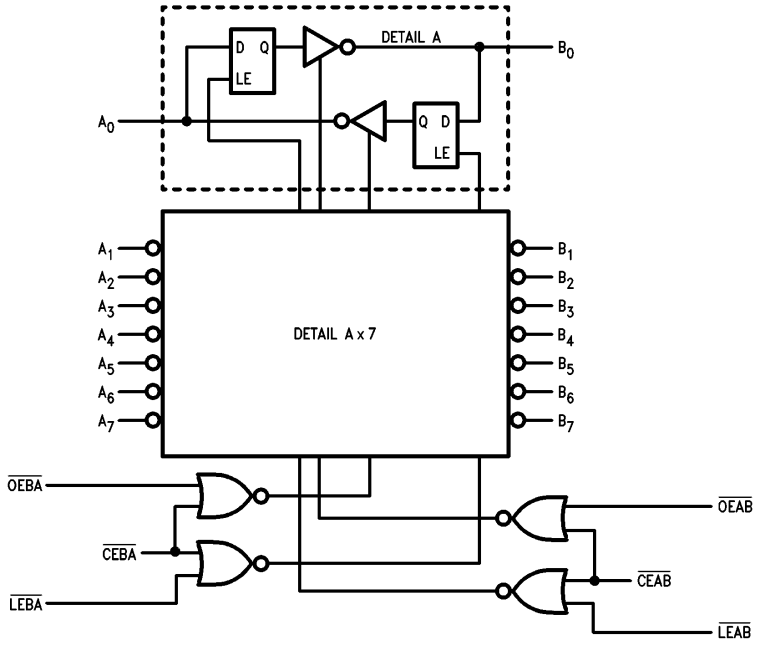
H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

A-to-B data flow shown; B-to-A flow control is the same, except using $\overline{CEBA}$, $\overline{LEBA}$ and $\overline{OEBA}$

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
TRI-STATE Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter		54F/74F Min	54F/74F Typ	54F/74F Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA, (except $\overline{A}_n$, $\overline{B}_n$)
V_{OH}	Output HIGH Voltage	54F 10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA ($\overline{A}_n$)
		54F 10% V_{CC}	2.4					I_{OH} = −3 mA ($\overline{A}_n$, $\overline{B}_n$)
		54F 10% V_{CC}	2.0					I_{OH} = −12 mA ($\overline{B}_n$)
		74F 10% V_{CC}	2.5					I_{OH} = −1 mA ($\overline{A}_n$)
		74F 10% V_{CC}	2.4					I_{OH} = −3 mA ($\overline{A}_n$, $\overline{B}_n$)
		74F 10% V_{CC}	2.0					I_{OH} = −15 mA ($\overline{B}_n$)
		74F 5% V_{CC}	2.7					I_{OH} = −1 mA ($\overline{A}_n$)
		74F 5% V_{CC}	2.7					I_{OH} = −3 mA ($\overline{A}_n$, $\overline{B}_n$)
V_{OL}	Output LOW Voltage	54F 10% V_{CC}			0.5	V	Min	I_{OL} = 20 mA ($\overline{A}_n$)
		54F 10% V_{CC}			0.55			I_{OL} = 48 mA ($\overline{B}_n$)
		74F 10% V_{CC}			0.5			I_{OL} = 24 mA ($\overline{A}_n$)
		74F 10% V_{CC}			0.55			I_{OL} = 64 mA ($\overline{B}_n$)
I_{IH}	Input HIGH Current	54F			20.0	μA	Max	V_{IN} = 2.7V (except $\overline{A}_n$, $\overline{B}_n$)
		74F			5.0			
I_{BVI}	Input HIGH Current Breakdown Test	54F			100	μA	Max	V_{IN} = 7.0V (except $\overline{A}_n$, $\overline{B}_n$)
		74F			7.0			
I_{BVIT}	Input HIGH Current Breakdown (I/O)	54F			1.0	mA	Max	V_{IN} = 5.5V ($\overline{A}_n$, $\overline{B}_n$)
		74F			0.5			
I_{CEX}	Output HIGH Leakage Current	54F			250	μA	Max	V_{OUT} = V_{CC} ($\overline{A}_n$, $\overline{B}_n$)
		74F			250			
V_{ID}	Input Leakage Test	74F	4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current	74F			3.75	μA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current				−0.6	mA	Max	V_{IN} = 0.5V ($\overline{OEAB}$, $\overline{OEBA}$)
					−1.2			V_{IN} = 0.5V ($\overline{CEAB}$, $\overline{CEBA}$)
I_{IH} + I_{OZH}	Output Leakage Current				70	μA	Max	V_{OUT} = 2.7V ($\overline{A}_n$, $\overline{B}_n$)
I_{IL} + I_{OZL}	Output Leakage Current				−650	μA	Max	V_{OUT} = 0.5V ($\overline{A}_n$, $\overline{B}_n$)

DC Electrical Characteristics (Continued)

Symbol	Parameter	54F/74F			Units	V_{CC}	Conditions
		Min	Typ	Max			
I_{OS}	Output Short-Circuit Current	−60 −100		−150 −225	mA	Max	V_{OUT} = 0V ($\overline{A}_n$) V_{OUT} = 0V ($\overline{B}_n$)
I_{ZZ}	Bus Drainage Test			500	μA	0.0V	V_{OUT} = 5.25V ($\overline{A}_n$, $\overline{B}_n$)
I_{CCH}	Power Supply Current		70	105	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current		85	130	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current		83	125	mA	Max	V_O = HIGH Z

AC Electrical Characteristics

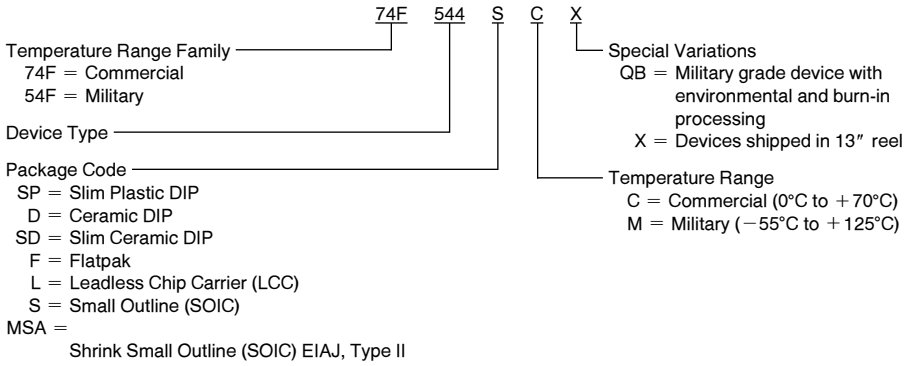
Symbol	Parameter	74F			54F		74F		Units
		T_A = +25°C V_{CC} = +5.0V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF		
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay Transparent Mode $\overline{A}_n$ to $\overline{B}_n$ or $\overline{B}_n$ to $\overline{A}_n$	3.0 3.0	7.0 5.0	9.5 6.5	3.0 2.5	12.0 8.5	3.0 3.0	10.5 7.5	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{LEBA}$ to $\overline{A}_n$	6.0 4.0	10.0 7.0	13.0 9.5	6.0 4.0	18.0 11.5	6.0 4.0	14.5 10.5	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{LEAB}$ to $\overline{B}_n$	6.0 4.0	10.0 7.0	13.0 9.5	6.0 4.0	18.0 11.5	6.0 4.0	14.5 10.5	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEBA}$ or $\overline{OEAB}$ to $\overline{A}_n$ or $\overline{B}_n$ $\overline{CEBA}$ or $\overline{CEAB}$ to $\overline{A}_n$ or $\overline{B}_n$	3.0 4.0	7.0 7.5	9.0 10.5	3.0 4.0	11.0 13.0	3.0 4.0	10.0 12.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEBA}$ or $\overline{OEAB}$ to $\overline{A}_n$ or $\overline{B}_n$ $\overline{CEBA}$ or $\overline{CEAB}$ to $\overline{A}_n$ or $\overline{B}_n$	1.0 2.5	6.0 5.5	8.0 10.5	2.0 2.0	10.0 9.5	1.0 2.5	9.0 11.5	

AC Operating Requirements

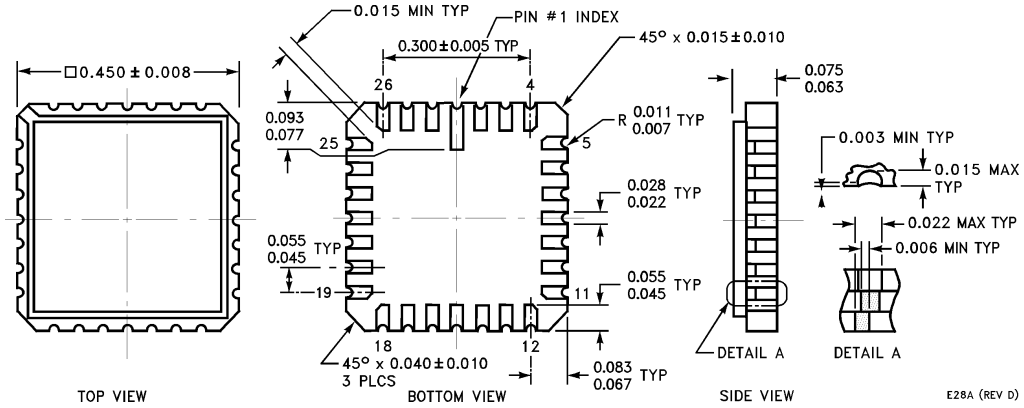
Symbol	Parameter	74F		54F		74F		Units
		T_A = +25°C V_{CC} = +5.0V		T_A, V_{CC} = Mil		T_A, V_{CC} = Com		
		Min	Max	Min	Max	Min	Max	
t_s(H) t_s(L)	Setup Time, HIGH or LOW $\overline{A}_n$ or $\overline{B}_n$ to $\overline{LEBA}$ or $\overline{LEAB}$	3.0 3.0		3.0 3.0		3.0 3.0		ns
t_h(H) t_h(L)	Hold Time, HIGH or LOW $\overline{A}_n$ or $\overline{B}_n$ to $\overline{LEBA}$ or $\overline{LEAB}$	3.0 3.0		3.0 3.0		3.0 3.0		
t_w(L)	Latch Enable, B to A Pulse Width, LOW	6.0		9.0		7.5		ns

Ordering Information

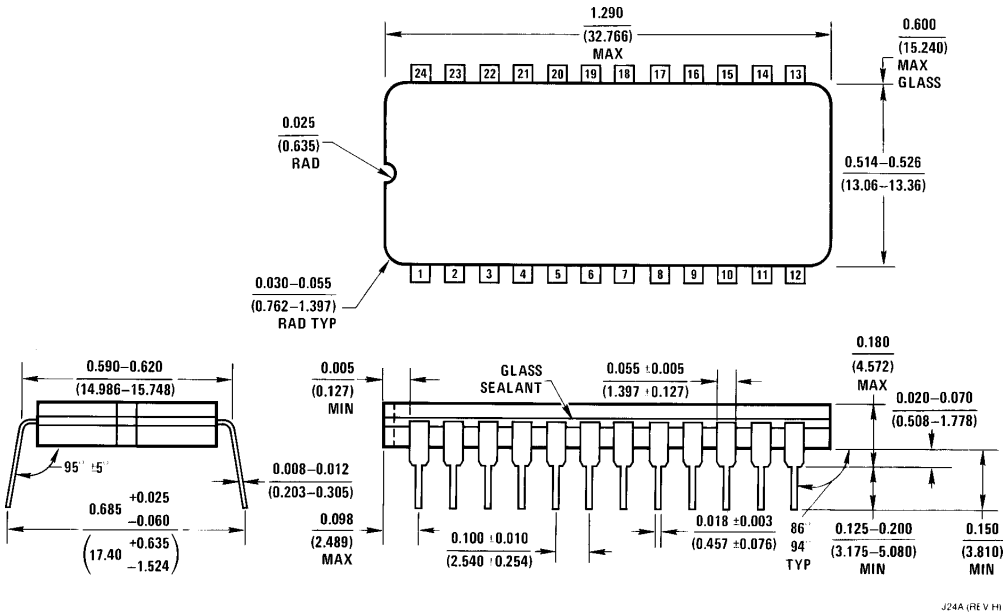
The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



Physical Dimensions inches (millimeters)

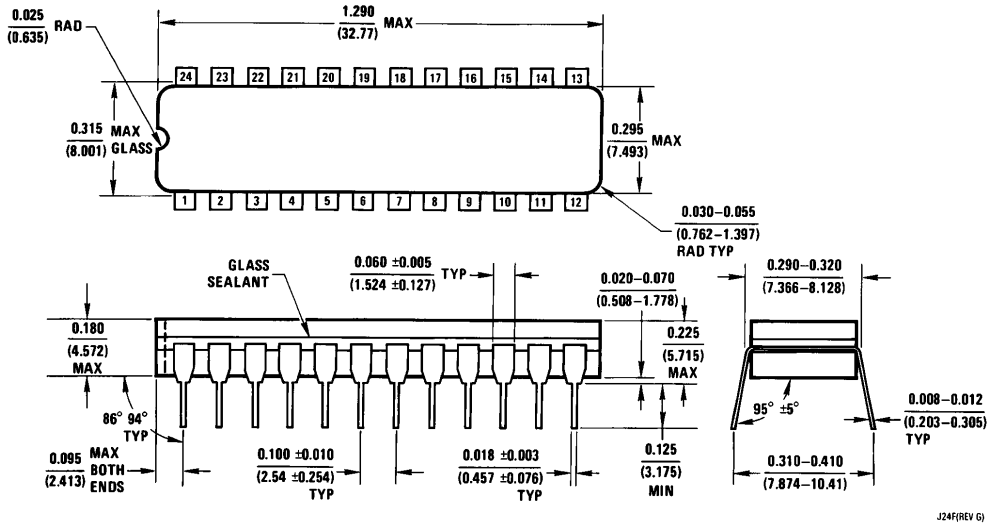


28-Lead Ceramic Leadless Chip Carrier (L)
NS Package Number E28A

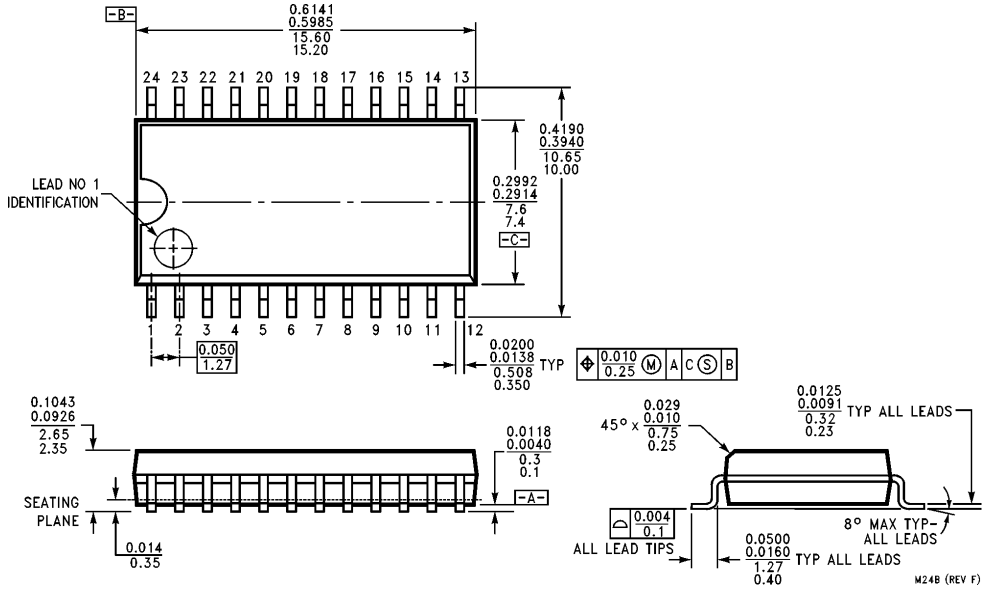


24-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J24A

Physical Dimensions inches (millimeters) (Continued)

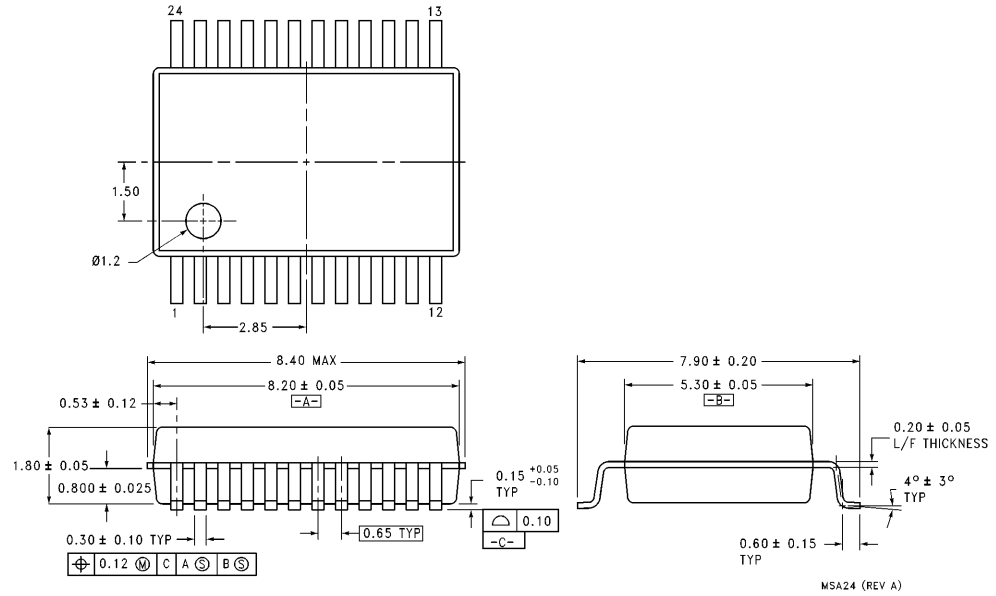


24-Lead (0.300″ Wide) Ceramic Dual-In-Line Package (SD)
NS Package Number J24F

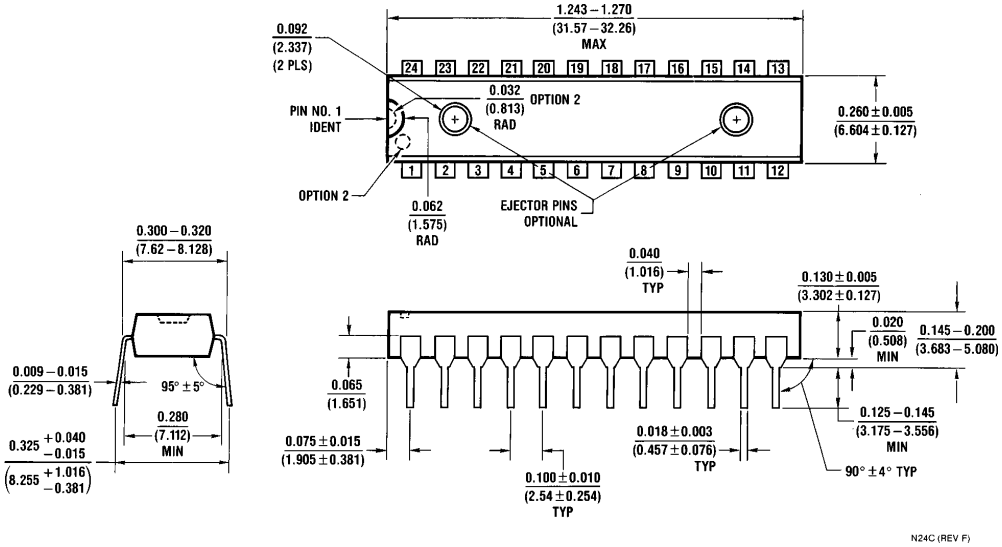


24-Lead (0.300″ Wide) Molded Small Outline Package, JEDEC (S)
NS Package Number M24B

Physical Dimensions inches (millimeters) (Continued)

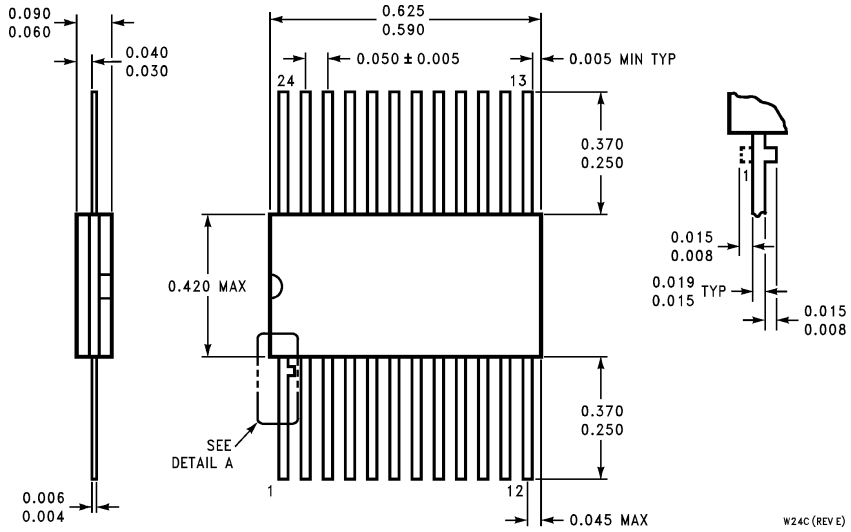


24-Lead Molded Shrink Small Outline, EIAJ, Type II (MSA)
NS Package Number MSA24



24-Lead (0.300″ Wide) Molded Dual-In-Line Package (SP)
NS Package Number N24C

Physical Dimensions inches (millimeters) (Continued)



24-Lead Ceramic Flatpak (F)
NS Package Number W24C

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