
HM6264BI Series

8,192-word × 8-bit High Speed CMOS Static RAM

HITACHI

ADE-203-492A (Z)

Rev. 1.0

Sep. 5, 1996

Description

The Hitachi HM6264BI is 64k-bit static RAM organized 8-kword × 8-bit. It realizes higher performance and low power consumption by 1.5 μm CMOS process technology. The device, packaged in 450 mil SOP (foot print pitch width), 600 mil plastic DIP, is available for high density mounting.

Features

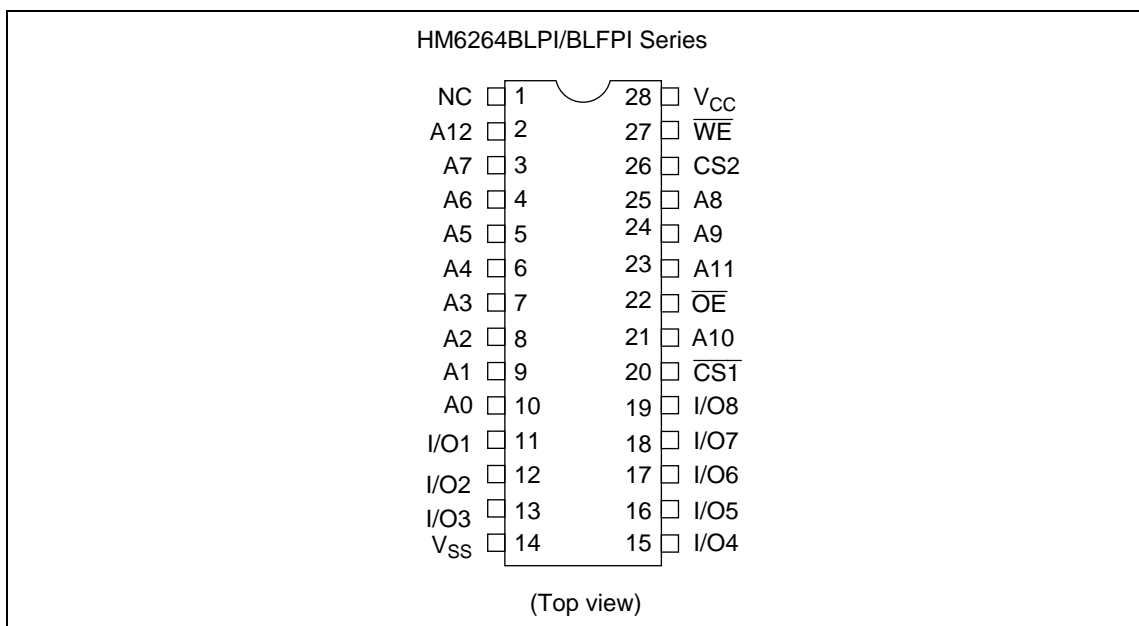
- High speed
 - Fast access time: 100/120 ns (max)
- Low power
 - Standby: 10 μW (typ)
 - Operation: 15 mW (typ) (f = 1 MHz)
- Single 5 V supply
- Completely static memory
 - No clock or timing strobe required
- Equal access and cycle times
- Common data input and output
 - Three state output
- Directly TTL compatible
 - All inputs and outputs
- Battery backup operation capability
- Operating temperature range
 - -40_C to +85_C

Ordering Information

Type No.	Access time	Package
HM6264BLPI-10	100 ns	600-mil, 28-pin plastic DIP (DP-28)
HM6264BLPI-12	120 ns	
HM6264BLFPI-10T	100 ns	450-mil, 28-pin plastic SOP(FP-28DA)
HM6264BLFPI-12T	120 ns	

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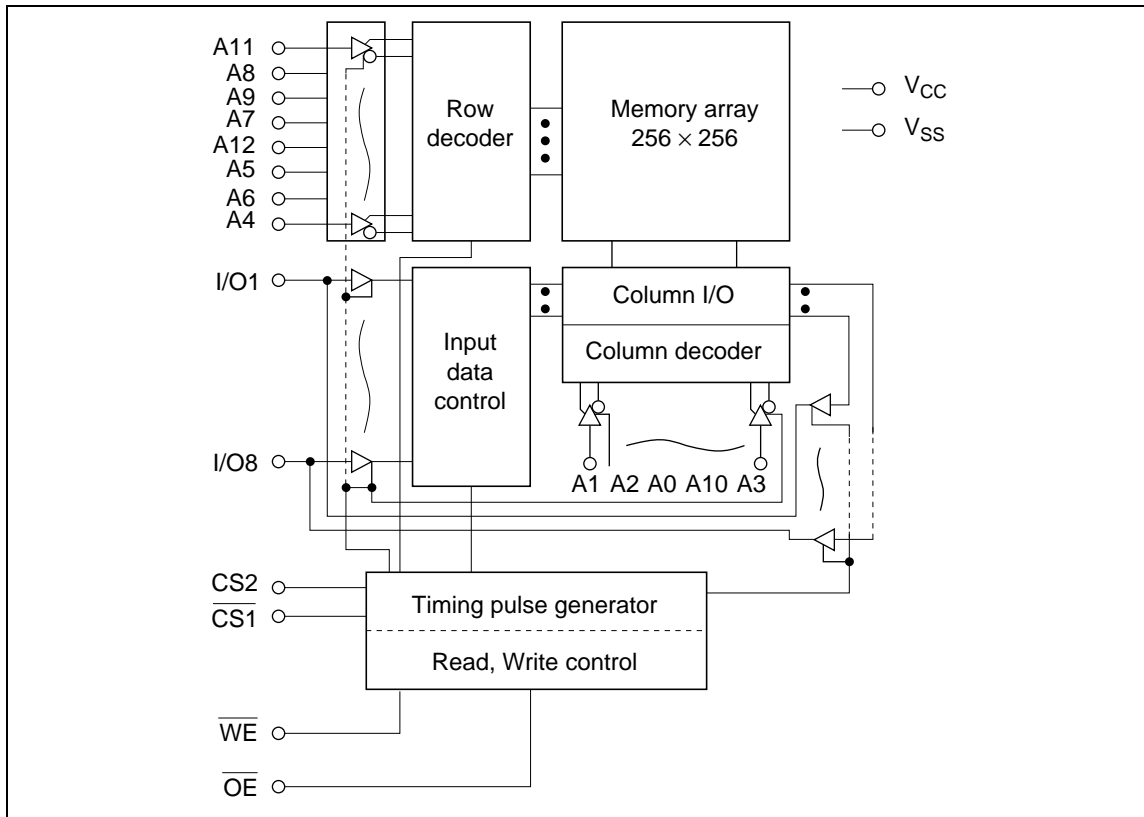
Pin Arrangement



Pin Description

Pin name	Function
A0 to A12	Address input
I/O1 to I/O8	Data input/output
CS1	Chip select 1
CS2	Chip select 2
WE	Write enable
OE	Output enable
NC	No connection
V _{cc}	Power supply
V _{ss}	Ground

Block Diagram



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Function Table

WE	CS1	CS2	OE	Mode	V _{CC} current	I/O pin	Ref. cycle
×	H	×	×	Not selected (power down)	I _{SB} , I _{SB1}	High-Z	—
×	×	L	×	Not selected (power down)	I _{SB} , I _{SB1}	High-Z	—
H	L	H	H	Output disable	I _{CC}	High-Z	—
H	L	H	L	Read	I _{CC}	Dout	Read cycle (1)–(3)
L	L	H	H	Write	I _{CC}	Din	Write cycle (1)
L	L	H	L	Write	I _{CC}	Din	Write cycle (2)

Note: ×: H or L

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage* ¹	V _{CC}	−0.5 to +7.0	V
Terminal voltage* ¹	V _T	−0.5* ² to V _{CC} + 0.3* ³	V
Power dissipation	P _T	1.0	W
Operating temperature	T _{opr}	−40 to +85	°C
Storage temperature	T _{stg}	−55 to +125	°C
Storage temperature under bias	T _{bias}	−40 to +85	°C

- Notes: 1. Relative to V_{SS}
 2. V_T min: −3.0 V for pulse half-width ² 50 ns
 3. Maximum voltage is 7.0 V

Recommended DC Operating Conditions (Ta = −40 to +85°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
	V _{SS}	0	0	0	V
Input high voltage	V _{IH}	2.4	—	V _{CC} + 0.3	V
Input low voltage	V _{IL}	−0.3* ¹	—	0.6	V

Note: 1. V_{IL} min: −3.0 V for pulse half-width ² 50 ns

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DC Characteristics (Ta = -40 to +85°C, V_{CC} = 5 V ±10%, V_{SS} = 0 V)

Parameter	Symbol	Min	Typ* ¹	Max	Unit	Test conditions
Input leakage current	I _{LI}	—	—	2	μA	V _{in} = V _{SS} to V _{CC}
Output leakage current	I _{LO}	—	—	2	μA	CS1 = V _{IH} or CS2 = V _{IL} or OE = V _{IH} or WE = V _{IL} , V _{I/O} = V _{SS} to V _{CC}
Operating power supply current	I _{CCDC}	—	7	20	mA	CS1 = V _{IL} , CS2 = V _{IH} , I _{I/O} = 0 mA others = V _{IH} /V _{IL}
Average operating power supply current	I _{CC1}	—	30	50	mA	Min cycle, duty = 100%, CS1 = V _{IL} , CS2 = V _{IH} , I _{I/O} = 0 mA others = V _{IH} /V _{IL}
	I _{CC2}	—	3	8	mA	Cycle time = 1 μs, duty = 100%, I _{I/O} = 0 mA CS1 ² 0.2 V, CS2 ³ V _{CC} - 0.2 V, V _{IH} ³ V _{CC} - 0.2 V, V _{IL} ² 0.2 V
Standby power supply current	I _{SB}	—	1	3	mA	CS1 = V _{IH} , CS2 = V _{IL}
	I _{SB1} ^{*2}	—	2	200	μA	CS1 ³ V _{CC} - 0.2 V, CS2 ³ V _{CC} - 0.2 V or 0 V ² CS2 ² 0.2 V, 0 V ² V _{in}
Output low voltage	V _{OL}	—	—	0.4	V	I _{OL} = 2.1 mA
Output high voltage	V _{OH}	2.4	—	—	V	I _{OH} = -1.0 mA

Notes: 1. Typical values are at V_{CC} = 5.0 V, Ta = +25°C and not guaranteed.

2. V_{IL} min = -0.3V

Capacitance (Ta = 25°C, f = 1.0 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance* ¹	C _{in}	—	—	5	pF	V _{in} = 0 V
Input/output capacitance* ¹	C _{I/O}	—	—	7	pF	V _{I/O} = 0 V

Note: 1. This parameter is sampled and not 100% tested.

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AC Characteristics ($T_a = -40$ to $+85^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$, unless otherwise noted.)

Test Conditions

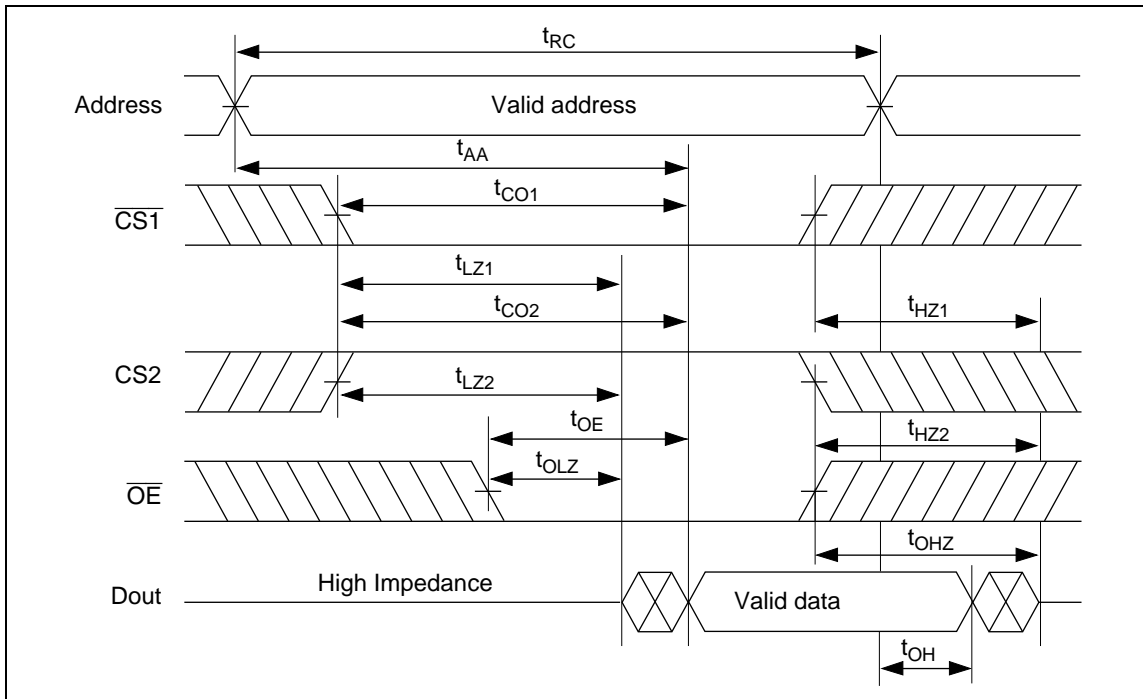
- Input pulse levels: 0.6 V to 2.4 V
- Input and output timing reference level: 1.5 V
- Input rise and fall time: 10 ns
- Output load: 1 TTL Gate + C_L (100 pF) (Including scope & jig)

Read Cycle

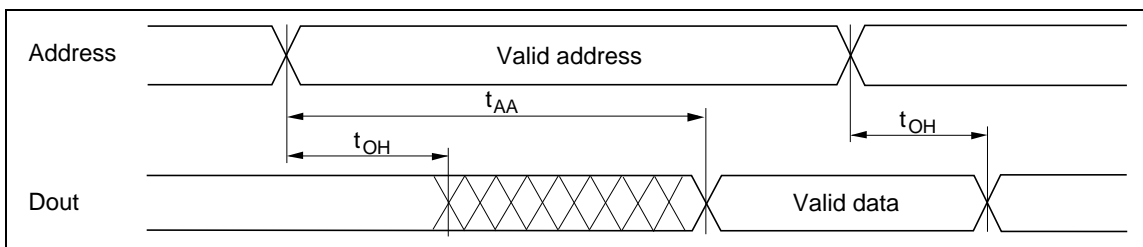
Parameter	Symbol	HM6264BI-10		HM6264BI-12		Unit	Notes
		Min	Max	Min	Max		
Read cycle time	t_{RC}	100	—	120	—	ns	
Address access time	t_{AA}	—	100	—	120	ns	
Chip select access time	CS1 t_{CO1}	—	100	—	120	ns	
	CS2 t_{CO2}	—	100	—	120	ns	
Output enable to output valid	t_{OE}	—	50	—	60	ns	
Chip selection to output in low-Z	CS1 t_{LZ1}	10	—	10	—	ns	2
	CS2 t_{LZ2}	10	—	10	—	ns	2
Output enable to output in low-Z	t_{OLZ}	5	—	5	—	ns	2
Chip deselection in to output in high-Z	CS1 t_{HZ1}	0	35	0	40	ns	1, 2
	CS2 t_{HZ2}	0	35	0	40	ns	1, 2
Output disable to output in high-Z	t_{OHZ}	0	35	0	40	ns	1, 2
Output hold from address change	t_{OH}	10	—	10	—	ns	

- Notes: 1. t_{HZ} is defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ} maximum is less than t_{LZ} minimum both for a given device and from device to device.
3. Address must be valid prior to or simultaneously with CS1 going low or CS2 going high.

Read Timing Waveform (1) ($\overline{WE} = V_{IH}$)

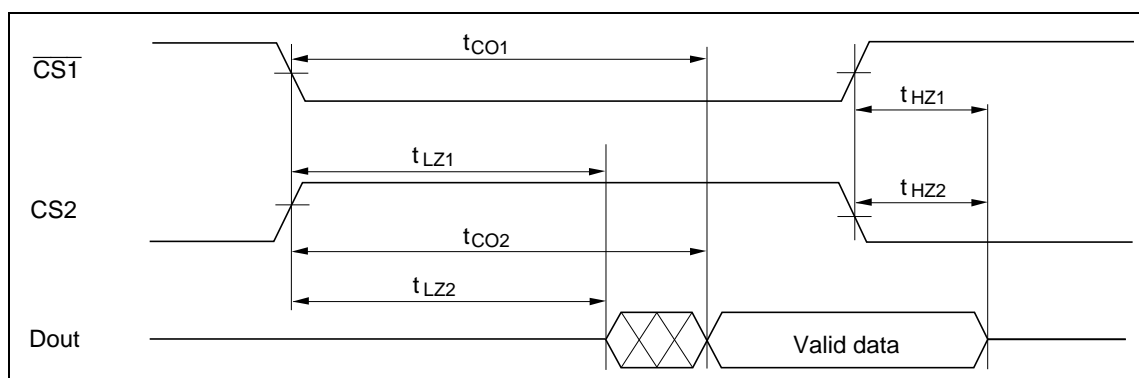


Read Timing Waveform (2) ($\overline{WE} = V_{IH}, \overline{OE} = V_{IL}$)



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Read Timing Waveform (3) ($\overline{WE} = V_{IH}$, $\overline{OE} = V_{IL}$)*³



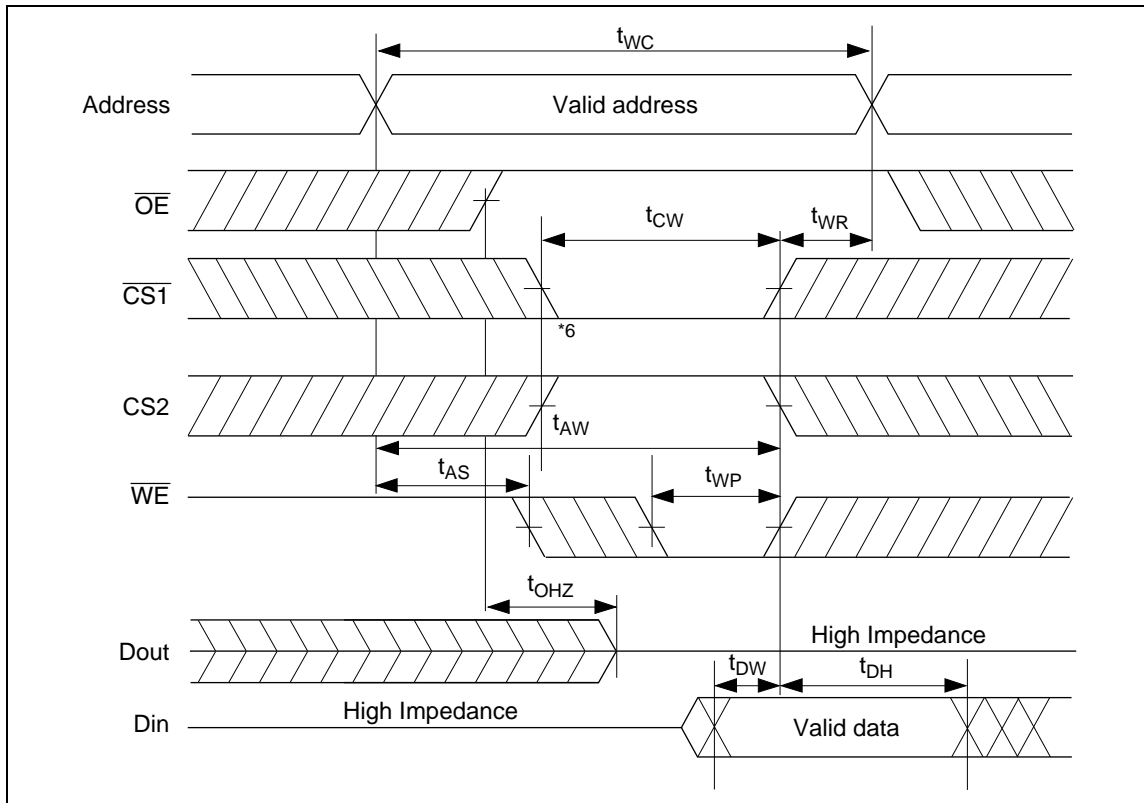
Write Cycle

Parameter	Symbol	HM6264BI-10		HM6264BI-12		Unit	Notes
		Min	Max	Min	Max		
Write cycle time	t_{WC}	100	—	120	—	ns	
Chip selection to end of write	t_{CW}	80	—	85	—	ns	2
Address setup time	t_{AS}	0	—	0	—	ns	3
Address valid to end of write	t_{AW}	80	—	85	—	ns	
Write pulse width	t_{WP}	60	—	70	—	ns	1, 9
Write recovery time	t_{WR}	0	—	0	—	ns	4
WE to output in high-Z	t_{WHZ}	0	35	0	40	ns	5
Data to write time overlap	t_{DW}	40	—	40	—	ns	
Data hold from write time	t_{DH}	0	—	0	—	ns	
Output active from end of write	t_{OW}	5	—	5	—	ns	
Output disable to output in high-Z	t_{OHZ}	0	35	0	40	ns	5

- Notes:
1. A write occurs during the overlap of a low CS1, and high CS2, and a high WE. A write begins at the latest transition among CS1 going low, CS2 going high and WE going low. A write ends at the earliest transition among CS1 going high, CS2 going low and WE going high. Time t_{WP} is measured from the beginning of write to the end of write.
 2. t_{CW} is measured from the later of CS1 going low or CS2 going high to the end of write.
 3. t_{AS} is measured from the address valid to the beginning of write.
 4. t_{WR} is measured from the earliest of CS1 or WE going high or CS2 going low to the end of write cycle.
 5. During this period, I/O pins are in the output state, therefore the input signals of the opposite phase to the outputs must not be applied.
 6. If CS1 goes low simultaneously with WE going low after WE goes low, the outputs remain in high impedance state.
 7. Dout is the same phase of the written data in this write cycle.
 8. Dout is the read data of the next address
 9. In the write cycle with OE low fixed, t_{WP} must satisfy the following equation to avoid a problem of data bus contention

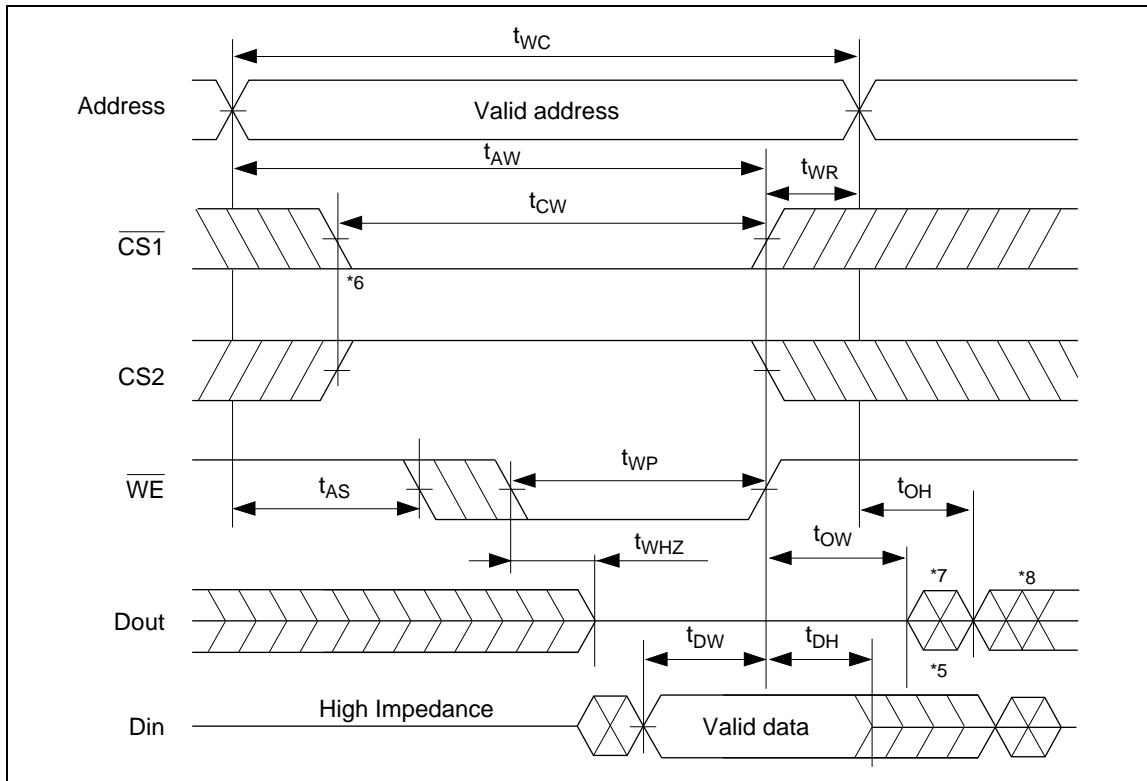
$$t_{WP} \geq t_{WHZ} \max + t_{DW} \min.$$

Write Timing Waveform (1) ($\overline{\text{OE}}$ Clock)



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Write Timing Waveform (2) (\overline{OE} Low Fixed) ($\overline{OE} = V_{IL}$)



Low V_{CC} Data Retention Characteristics ($T_a = -40$ to $+85^\circ\text{C}$)

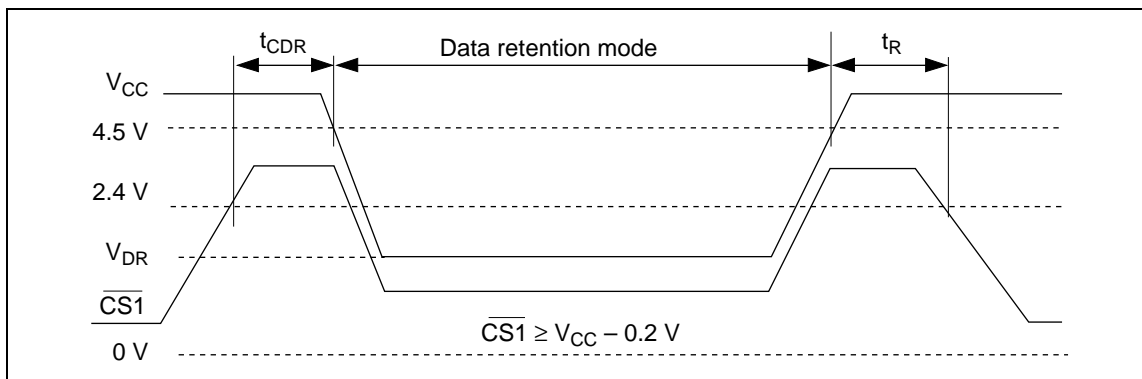
Parameter	Symbol	Min	Typ* ¹	Max	Unit	Test conditions* ³
V_{CC} for data retention	V_{DR}	2.0	—	—	V	CS1 ³ $V_{CC} - 0.2$ V, CS2 ³ $V_{CC} - 0.2$ V or CS2 ² 0.2 V Vin ³ 0 V
Data retention current	I_{CCDR}	—	1* ¹	100* ²	μA	$V_{CC} = 3.0$ V, 0 V ² Vin ² V_{CC} CS1 ³ $V_{CC} - 0.2$ V, CS2 ³ $V_{CC} - 0.2$ V or 0 V ² CS2 ² 0.2 V
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t_R	5	—	—	ms	

Notes: 1. Reference data at $T_a = 25^\circ\text{C}$.

2. V_{IL} min = -0.3 V.

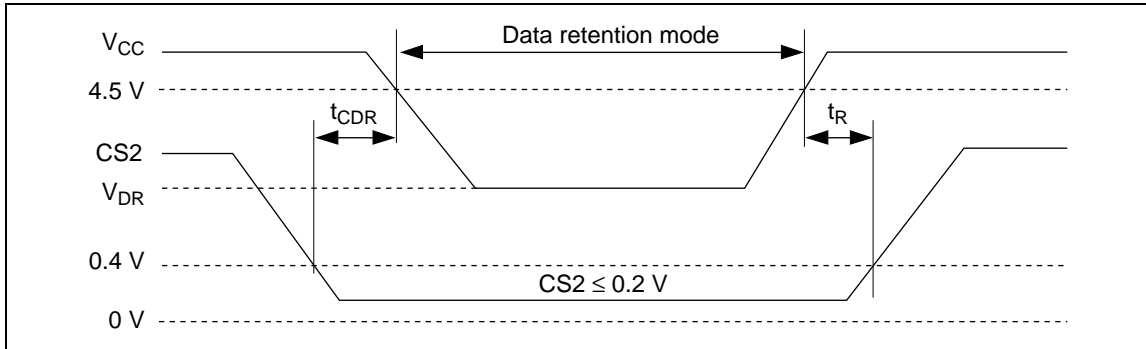
3. CS2 controls address buffer, WE buffer, CS1 buffer, OE buffer, and Din buffer. If CS2 controls data retention mode, Vin levels (address, WE, OE, CS1, I/O) can be in the high impedance state. If CS1 controls data retention mode, CS2 must be CS2 ³ $V_{CC} - 0.2$ V or 0 V ² CS2 ² 0.2 V. The other input levels (address, WE, OE, I/O) can be in the high impedance state.

Low V_{CC} Data Retention Timing Waveform (1) ($\overline{\text{CS1}}$ Controlled)



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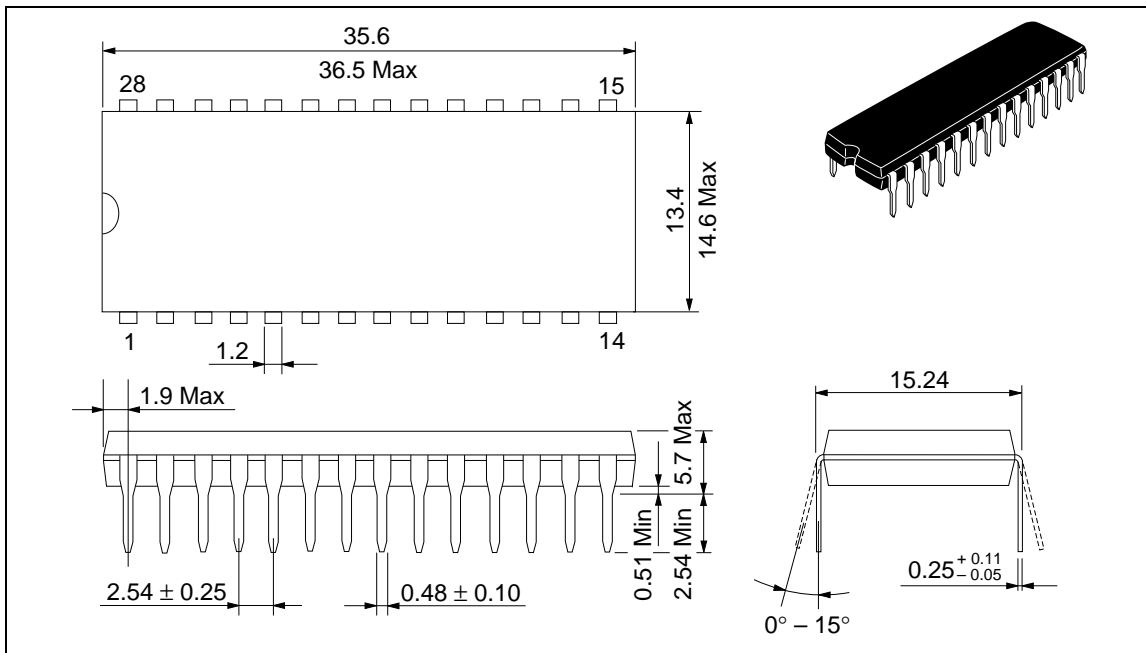
Low V_{CC} Data Retention Timing Waveform (2) (CS2 Controlled)



Package Dimensions

HM6264BLFPI Series (DP-28)

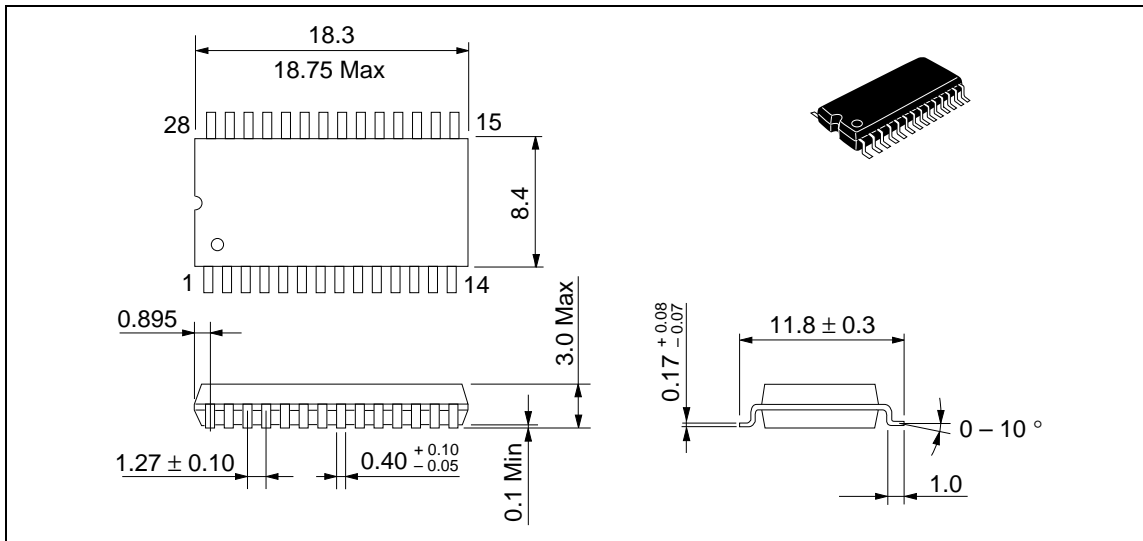
Unit: mm



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HM6264BLPI Series (FP-28DA)

Unit: mm



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Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.0	Dec. 1, 1995	Initial issue	I. Ogiwara	K. Yoshizaki
1.0	Sep. 5, 1996	Deletion of Preliminary		
