SX18AC75/SX20AC75/SX28AC75/SX20AC100/SX28AC100

High-Performance 8-Bit Microcontrollers with EE/Flash Program Memory and In-System Programming Capability

1.0 PRODUCT OVERVIEW

1.1 Introduction

The SX18AC75, SX20AC75, SX28AC75, SX20AC100 and SX28AC100 are members of the SX family of high-performance 8-bit microcontrollers fabricated in an advanced CMOS process technology. The advanced process, combined with a RISC-based architecture, allows high-speed computation, flexible I/O control, and efficient data manipulation. Throughput is enhanced by operating the device at frequencies up to 100MHz and by optimizing the instruction set to include mostly single-cycle instructions.

On-chip functions include a general-purpose 8-bit timer with prescaler, an analog comparator, a brown-out detector, a watchdog timer, a power-save mode with multi-source wakeup capability, an internal R/C oscillator, user-selectable clock modes, and high-current outputs.

1.2 Key Features

- 75 MIPS performance at 75 MHz oscillator frequency (SX18/20/28AC75)
- 100 MIPS performance at 100 MHz oscillator frequency (SX20/28AC100)
- 2048 x 12 bits EE/Flash program memory rated for 10,000 rewrite cycles
- 136 x 8 bits SRAM
- In-system programming capability through OSC pins
- Internal RC oscillator with configurable rate from 31.25 KHz to 4 MHz, ±8% accuracy (continued on page 2)

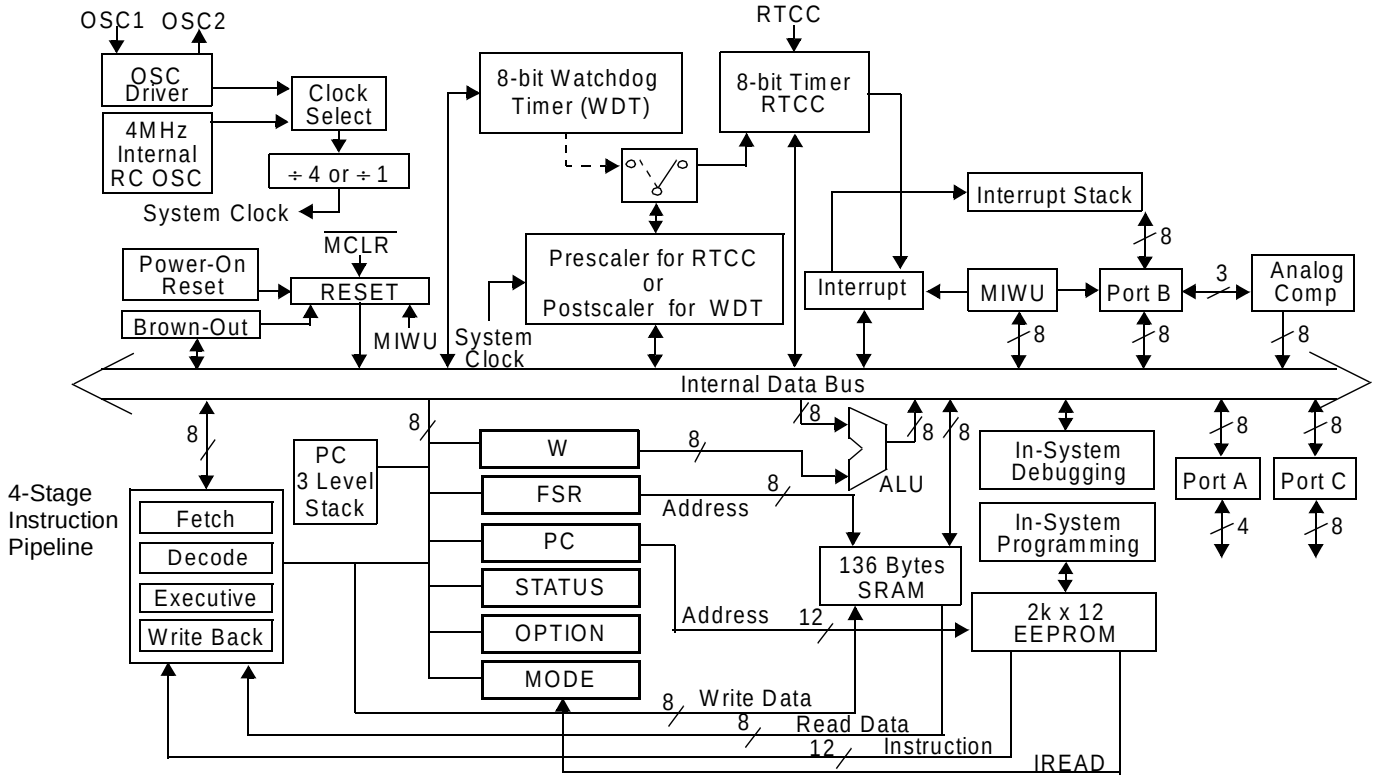

Figure 1-1. Block Diagram

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1.2 Key Features (Continued)

- User selectable clock modes:
  - Internal RC oscillator
  - External oscillator
  - Crystal/resonator options
- External RC oscillator
- Analog comparator
- Brown-out detector (4.2V, on/off)
- Multi-Input Wakeup (MIWU) on eight pins
- Fast lookup capability through run-time readable code
- Complete development tool support available through Parallax

1.2.1 CPU Features

- Fully static design – DC to 100 MHz operation
- Fast instruction cycle time
  - 13.3 ns (SX18/20/28AC75)
  - 10 ns (SX20/28AC100)
- Mostly single-cycle instructions
- Selectable 8-level deep hardware subroutine stack
- Single-level interrupt stack
- Fixed three-cycle interrupt response time
- Hardware context save/restore for interrupt
- Designed to be pin-compatible and upward code-compatible with the PIC165x®

1.2.2 I/O Features

- Software-selectable I/O configuration
  - Each pin programmable as an input or output
  - TTL or CMOS level selection on inputs
  - Internal weak pull-up selection on inputs (~20 kΩ to V_{dd})
- Schmitt trigger inputs on Port B and Port C
- All outputs capable of sinking/sourcing 30 mA
- Symmetrical drive on Port A outputs (same V_{drop} +/-)

1.3 Architecture

The SX devices use a modified Harvard architecture. This architecture uses two separate memories with separate address buses, one for the program and one for data, while allowing transfer of data from program memory to SRAM. This ability allows accessing data tables from program memory. The advantage of this architecture is that instruction fetch and memory transfers can be overlapped with a multi-stage pipeline, which means the next instruction can be fetched from program memory while the current instruction is being executed using data from the data memory.

The SX family implements a four-stage pipeline (fetch, decode, execute, and write back), which results in execution of one instruction per clock cycle. At the maximum operating frequency of 100 MHz, instructions are executed at the rate of one per 10-ns clock cycle.

1.4 Programming and Debugging Support

The SX devices are currently supported by the SX-Key™ offered by Parallax, Inc. This tool provides an integrated development environment including editor, macro assembler, debugger, and programmer.

1.5 Applications

Emerging applications and advances in existing ones require higher performance while maintaining low cost and fast time-to-market.

The SX devices provide solutions for many familiar applications such as process controllers, electronic appliances/tools, security/monitoring systems, digital filter implementation, high speed video processing, and telecommunication devices such as a FSK modems with DTMF generation/detection and Caller ID function. With 75 MHz or 100 MHz performance, the SX devices can even replace FPGAS, PLDs, and DSP functions. The deterministic executive of time-critical functions allows efficient implementation of real-time kernels. In addition, the enhanced throughput allows efficient development of software modules called Virtual Peripherals to replace on-chip hardware peripherals. The concept of Virtual Peripherals provides benefits such as using a more simple device, reduced component count, fast time to market, increased flexibility in design, and ultimately overall system cost reduction.

Some examples of Virtual Peripheral modules are:

- Serial, Parallel, I^2C™, Microwire™ (µ-Wire), Dallas µ-Wire, SPI, DMX-512, X-10, IR transceivers
- Frequency generation and measurement
- Spectrum analysis
- Multi-tasking, interrupts, and networking
- Resonance loops
- DRAM drivers
- Music and voice synthesis
- PPM/PWM output
- Delta/Sigma ADC
- DTMF I/O and call progress
- 300/1200 baud modem
- Quadrature encoder/decoder
- Peripheral Interface Device (PID) and servo control
- Video controller

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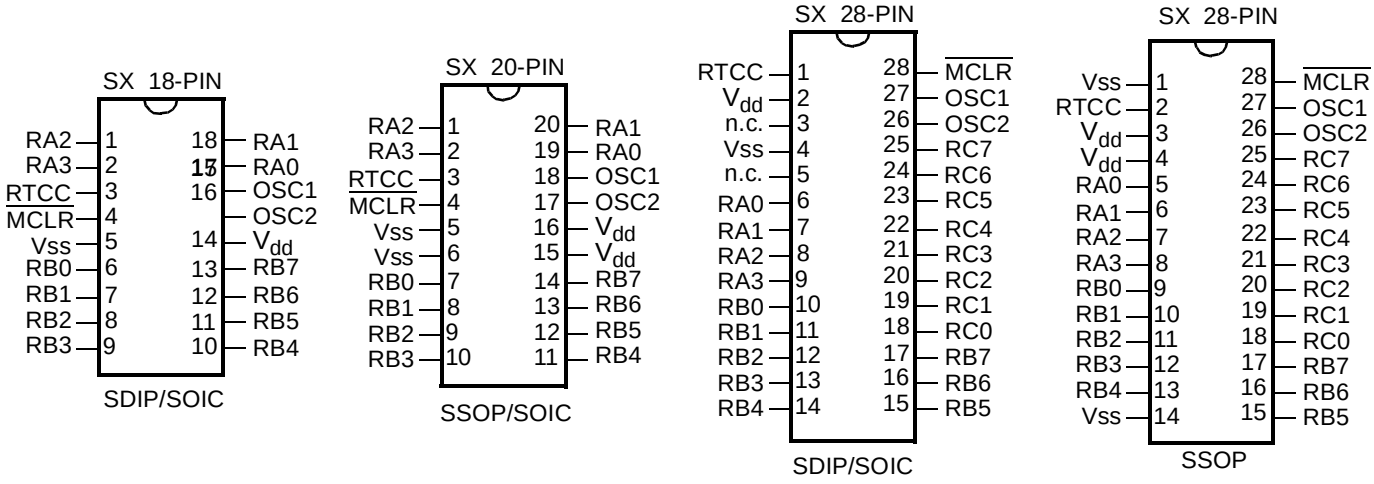
2.0 CONNECTION DIAGRAMS

2.1 Pin Assignments



2.2 Pin Descriptions

Name	Pin Type	Input Levels	Description
RA0	I/O	TTL/CMOS	Bidirectional I/O Pin; symmetrical source / sink capability
RA1	I/O	TTL/CMOS	Bidirectional I/O Pin; symmetrical source / sink capability
RA2	I/O	TTL/CMOS	Bidirectional I/O Pin; symmetrical source / sink capability
RA3	I/O	TTL/CMOS	Bidirectional I/O Pin; symmetrical source / sink capability
RB0	I/O	TTL/CMOS/ST	Bidirectional I/O Pin; comparator output; MIWU input
RB1	I/O	TTL/CMOS/ST	Bidirectional I/O Pin; comparator negative input; MIWU input
RB2	I/O	TTL/CMOS/ST	Bidirectional I/O Pin; comparator positive input; MIWU input
RB3	I/O	TTL/CMOS/ST	Bidirectional I/O Pin; MIWU input
RB4	I/O	TTL/CMOS/ST	Bidirectional I/O Pin; MIWU input
RB5	I/O	TTL/CMOS/ST	Bidirectional I/O Pin; MIWU input
RB6	I/O	TTL/CMOS/ST	Bidirectional I/O Pin; MIWU input
RB7	I/O	TTL/CMOS/ST	Bidirectional I/O Pin; MIWU input
RC0	I/O	TTL/CMOS/ST	Bidirectional I/O pin
RC1	I/O	TTL/CMOS/ST	Bidirectional I/O pin
RC2	I/O	TTL/CMOS/ST	Bidirectional I/O pin
RC3	I/O	TTL/CMOS/ST	Bidirectional I/O pin
RC4	I/O	TTL/CMOS/ST	Bidirectional I/O pin
RC5	I/O	TTL/CMOS/ST	Bidirectional I/O pin
RC6	I/O	TTL/CMOS/ST	Bidirectional I/O pin
RC7	I/O	TTL/CMOS/ST	Bidirectional I/O pin
RTCC	I	ST	Input to Real-Time Clock/Counter
$\overline{MCLR}$	I	ST	Master Clear reset input – active low
OSC1/In/Vpp	I	ST	Crystal oscillator input – external clock source input
OSC2/Out	O	CMOS	Crystal oscillator output – in R/C mode, internally pulled to V_{dd} through weak pull-up
V_{dd}	P	–	Positive supply pin
Vss	P	–	Ground pin
Note:I = input, O = output, I/O = Input/Output, P = Power, TTL = TTL input, CMOS = CMOS input, ST = Schmitt Trigger input, MIWU = Multi-Input Wakeup input			

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2.3 Part Numbering

Table 2-1. Ordering Information

Device	Pins	I/O	EE/Flash (Words)	RAM (Bytes)
SX18AC75/SO	18	12	2K	136
SX18AC75/DP	18	12	2K	136
SX20AC75/SS	20	12	2K	136
SX20AC100/SO	20	12	2K	136
SX28AC75/SO	28	20	2K	136
SX28AC75/DP	28	20	2K	136
SX28AC75/SS	28	20	2K	136
SX28AC100/SO	28	20	2K	136

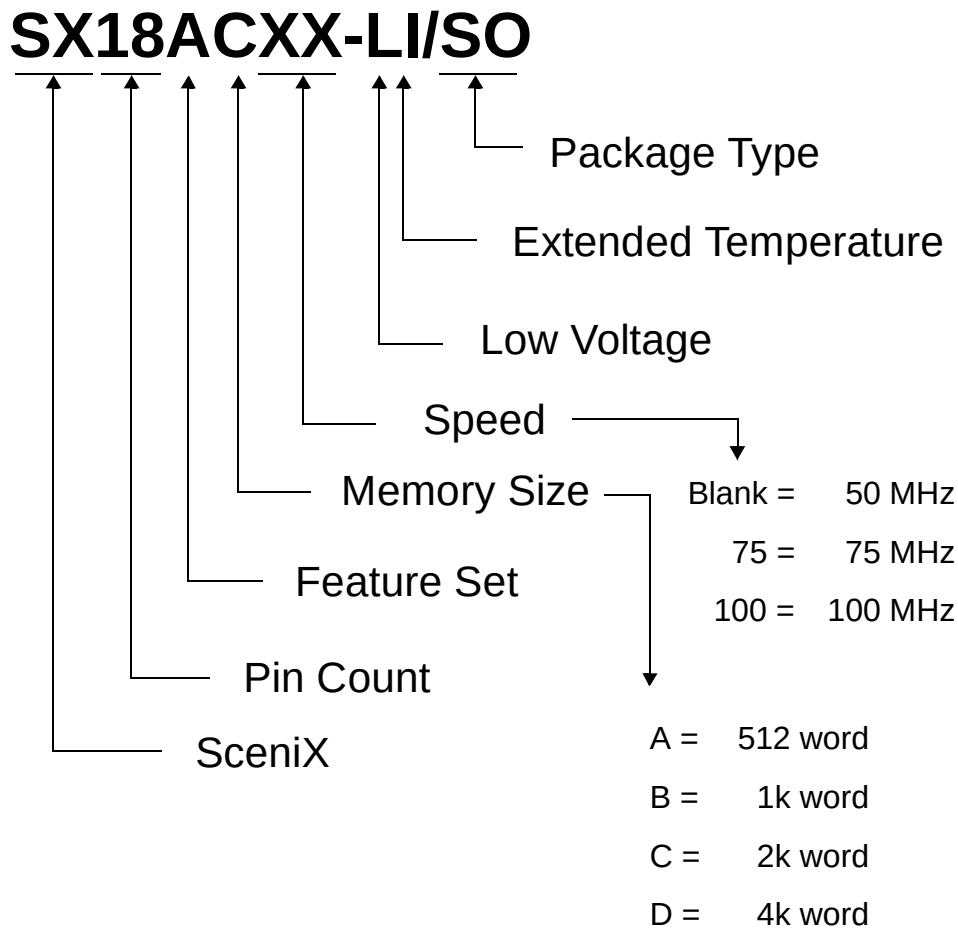

Figure 2-1. Part Number Reference Guide

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For the latest contact and support information on SX devices, please visit the Scenix Semiconductor website at www.scenix.com. The site contains technical literature, local sales contacts, tech support and many other features.

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